EGC220
Class Notes
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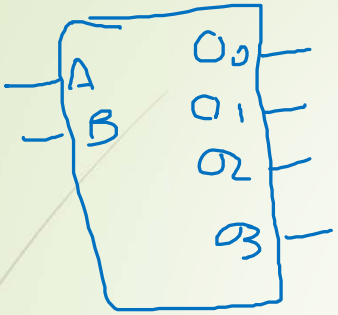
Final:

Closed book and notes

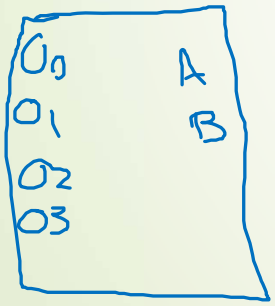
- Number systems
- Simplification using K-map
  - SOP, POS, Standard SOP and POS, Min. SOP and POS
- Design of combinational circuits
- Circuit conversion to all NAND or NOR gates
- Multiplexers, Demultiplexers, Decoders, Encoders
- Design of combinational circuits using PLD's
- Latch and flip flops characteristics and excitation tables, design of ripple counters
- Analysis of sequential circuits
- Design of sequential circuits
  - Design using Mealy and Moore model
  - Design of a sequence detector
  - Design of a shift register
  - Design of a controller

Decoder



A	B	O_3	O_2	O_1	O_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Priority Encoder



highest			lowest			
O_3	O_2	O_1	O_0	A	B	V
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

$A = O_3 + O_2$

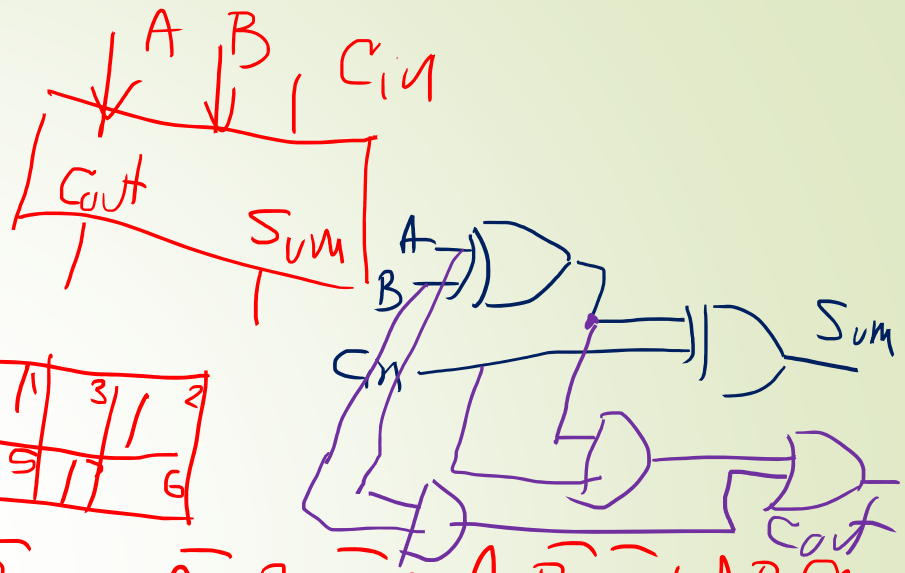
$B = O_3 + O_1$

$\overline{V} = \overline{O_3}\,\overline{O_2}\,\overline{O_1}\,\overline{O_0}$

$V = O_3 + O_2 + O_1 + O_0$

Full Adder

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



$$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

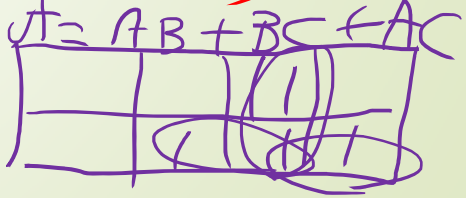
$$\bar{A}(\bar{B}C + B\bar{C}) + A(\overline{\bar{B}C} + B\bar{C})$$

$$\bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$C_{in}(A \oplus B) + AB(\bar{C} + C)$$



8 bits

	unsigned	Signed Mag	Signed 2's comp
42.5	01010101	01010101	01010101
-42.5	~~X~~	11010101	10101011

5

64 32 16 8 4 2 1 .5

0 1 0 1 0 1 0 .1

-01010101

10101011

128 64 32 16 8 4 2 1

11010011

what domain

a. unsigned → 211

b. Signed Mag.

64 32 16 8 4 2 1

11010011

neg. -83

c. Signed 2's comp

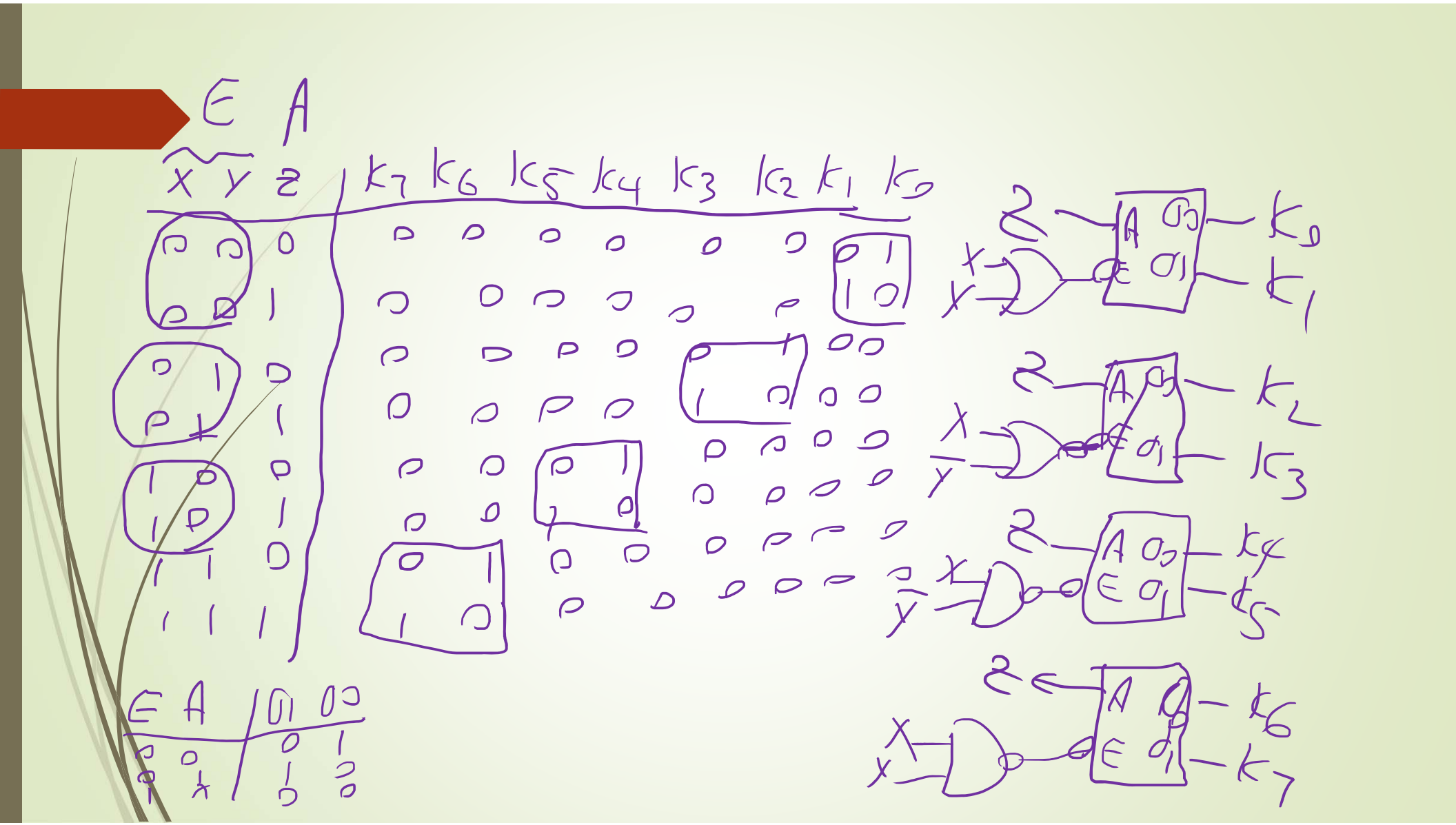
neg.

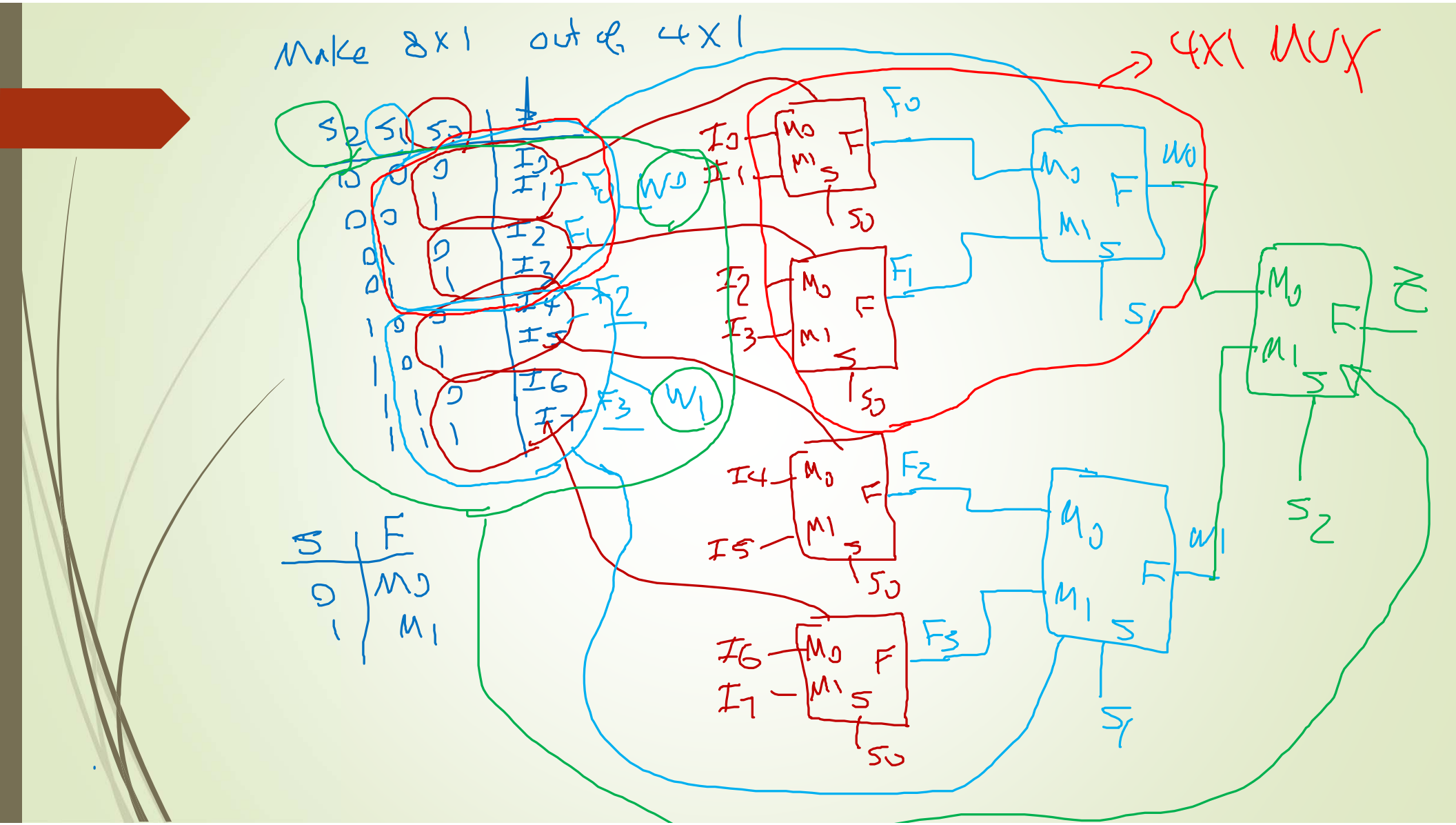
11010011

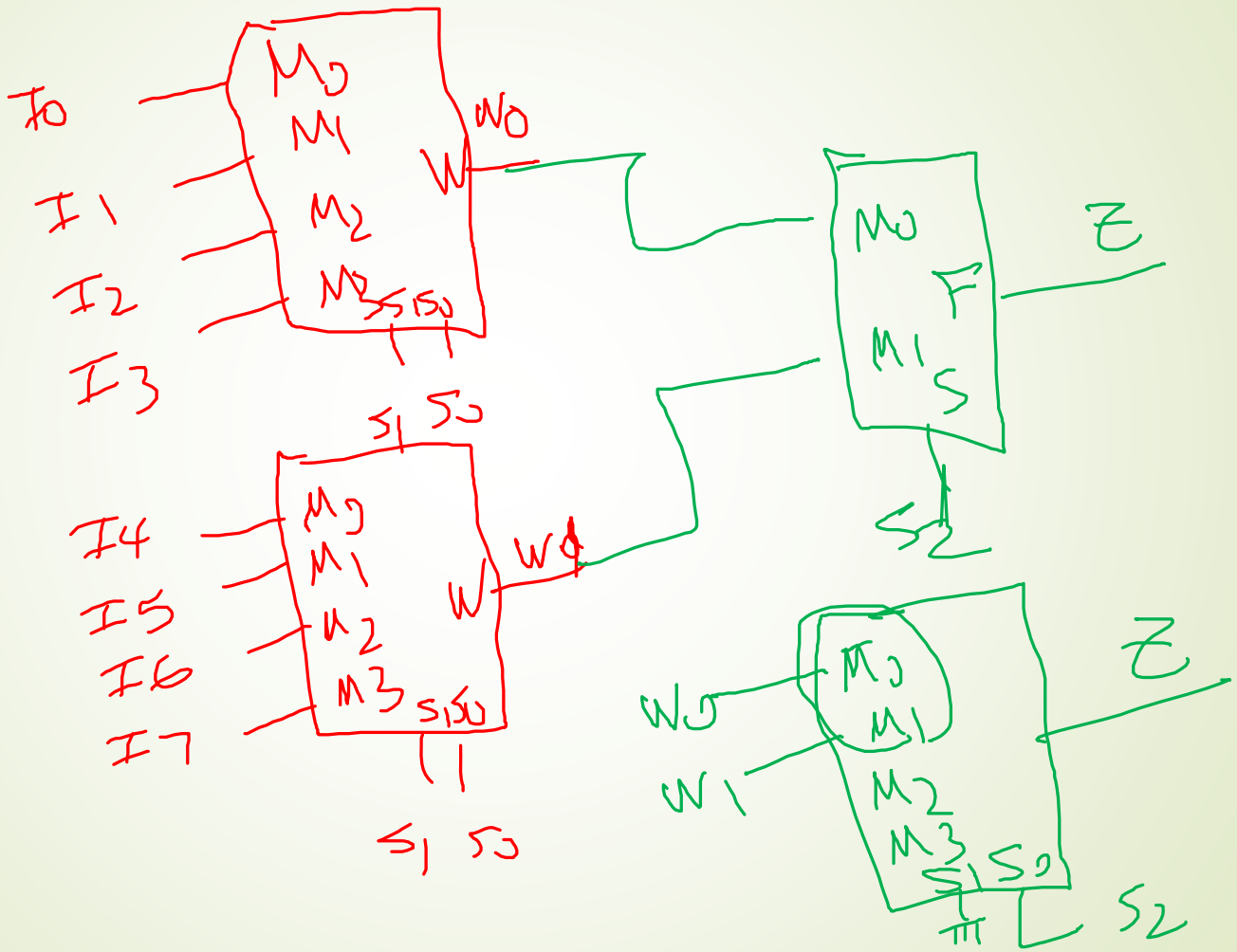
-00101101

32 16 8 4 2 1

-45


EA
x y z
k7 k6 k5 k4 k3 k2 k1 k0
EA | O1 O0
z
x
y
A
E
O0
O1
k0
k1
k2
k3
k4
k5
k6
k7


Make 8x1 out of 4x1
4x1 MUX
S2 S1 S0
I0 I1 I2 I3 I4 I5 I6 I7
F0 F1 F2 F3
W0 W1
M0 M1 S F
S0 S1 S2
S F
0 M0
1 M1


I0
I1
I2
I3
M0
M1
M2
M3
S1 S0
W0
W
S1 S0
I4
I5
I6
I7
M0
M1
M2
M3
S1,S0
W1
W
S1 S0
M0
F
M1
S
Z
S2
W0
W1
M0
M1
M2
M3
S1 S0
Z
S2

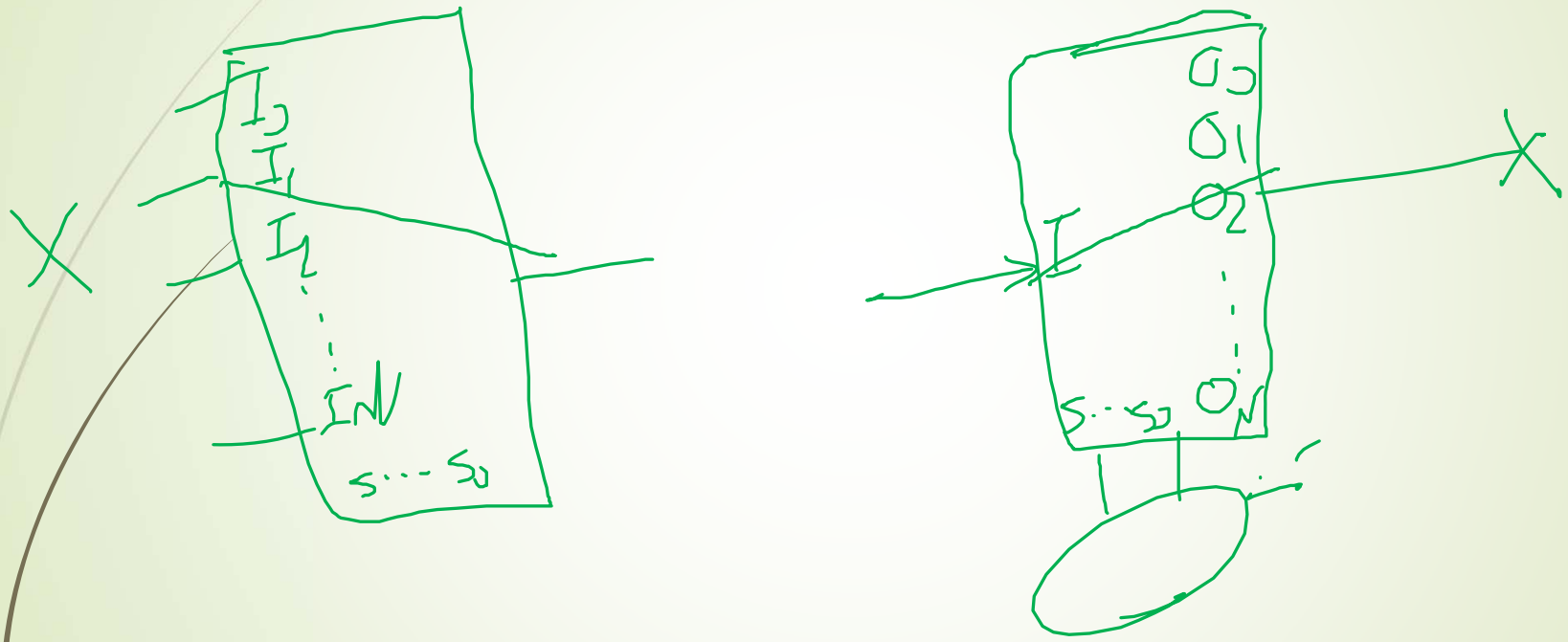
8X1 MUX

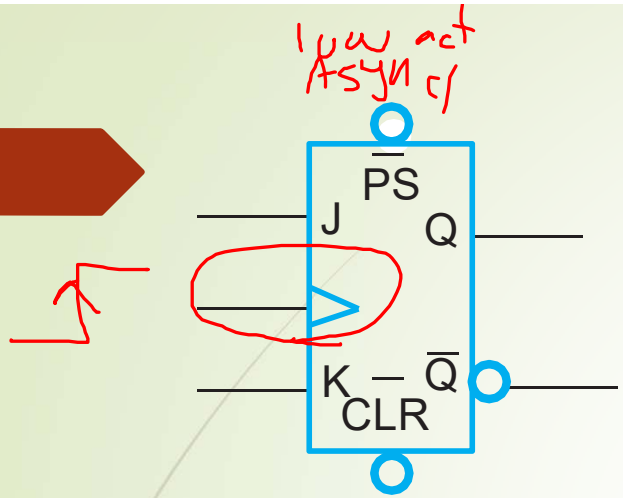
$F = \Sigma m(4, 6, 9, 13, 15)$

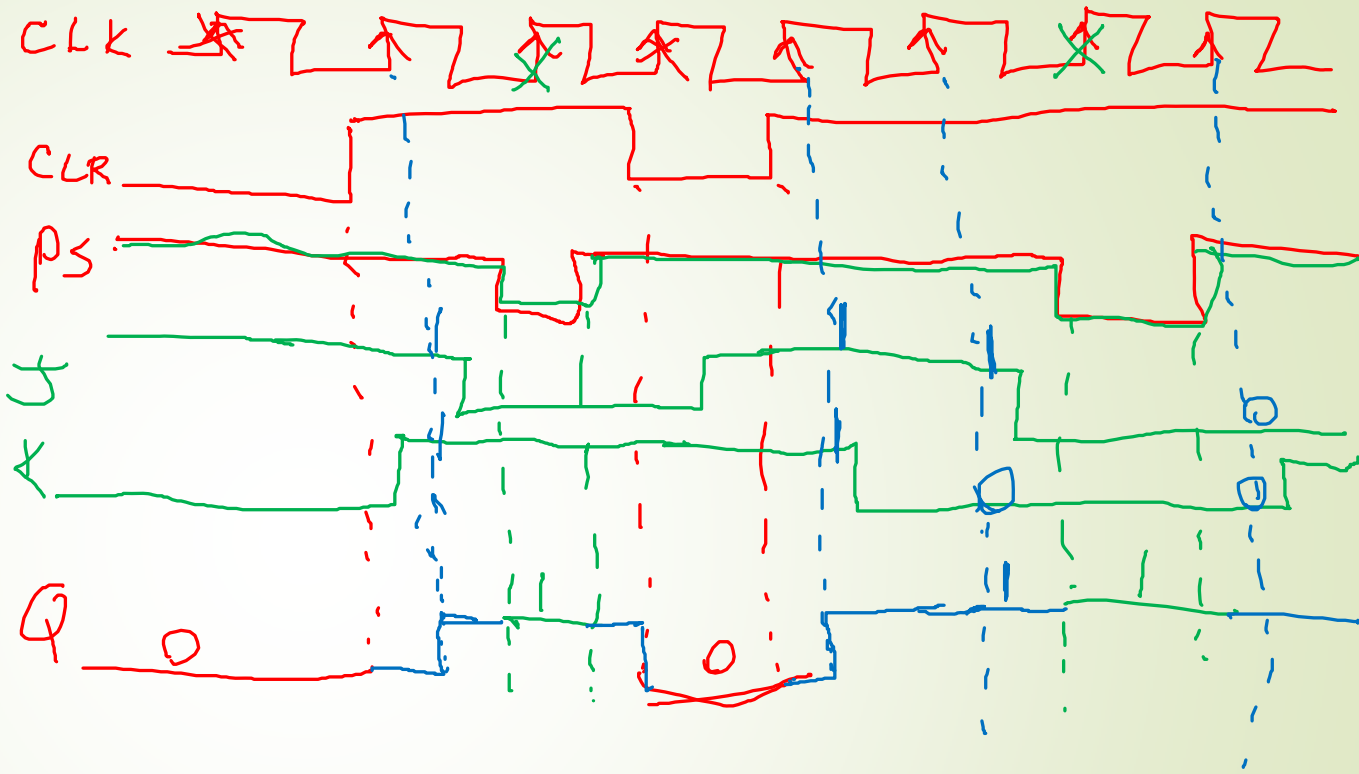
S_2	S_1	S_0	Z
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

$Z = \bar{S}_2\bar{S}_1\bar{S}_0 I_0 + \bar{S}_2\bar{S}_1 S_0 I_1 + \bar{S}_2 S_1\bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3 + S_2\bar{S}_1\bar{S}_0 I_4 + S_2\bar{S}_1 S_0 I_5 + S_2 S_1\bar{S}_0 I_6 + S_2 S_1 S_0 I_7$

4X1 MUX


I0
I1
IN
S ... S0
X
O0
O1
O2
ON
S ... S0
X


low act
Asynch
PS
J
Q
K
CLR
Q
low
act.
Asynch


CLK
CLR
PS
J
K
Q
0
0
1
0
0

sequence overlapping Moore

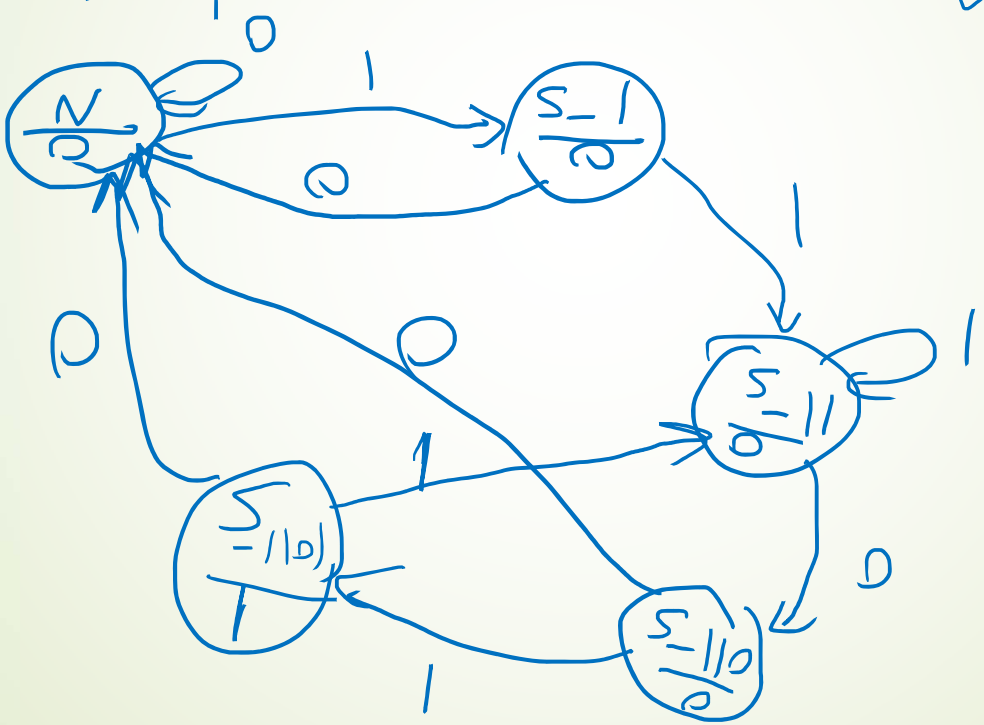
1101101

1101

10

11100

z



N = nothing

S_1 : 1 detected

S_11 : 11 "

S_110 : 110 "

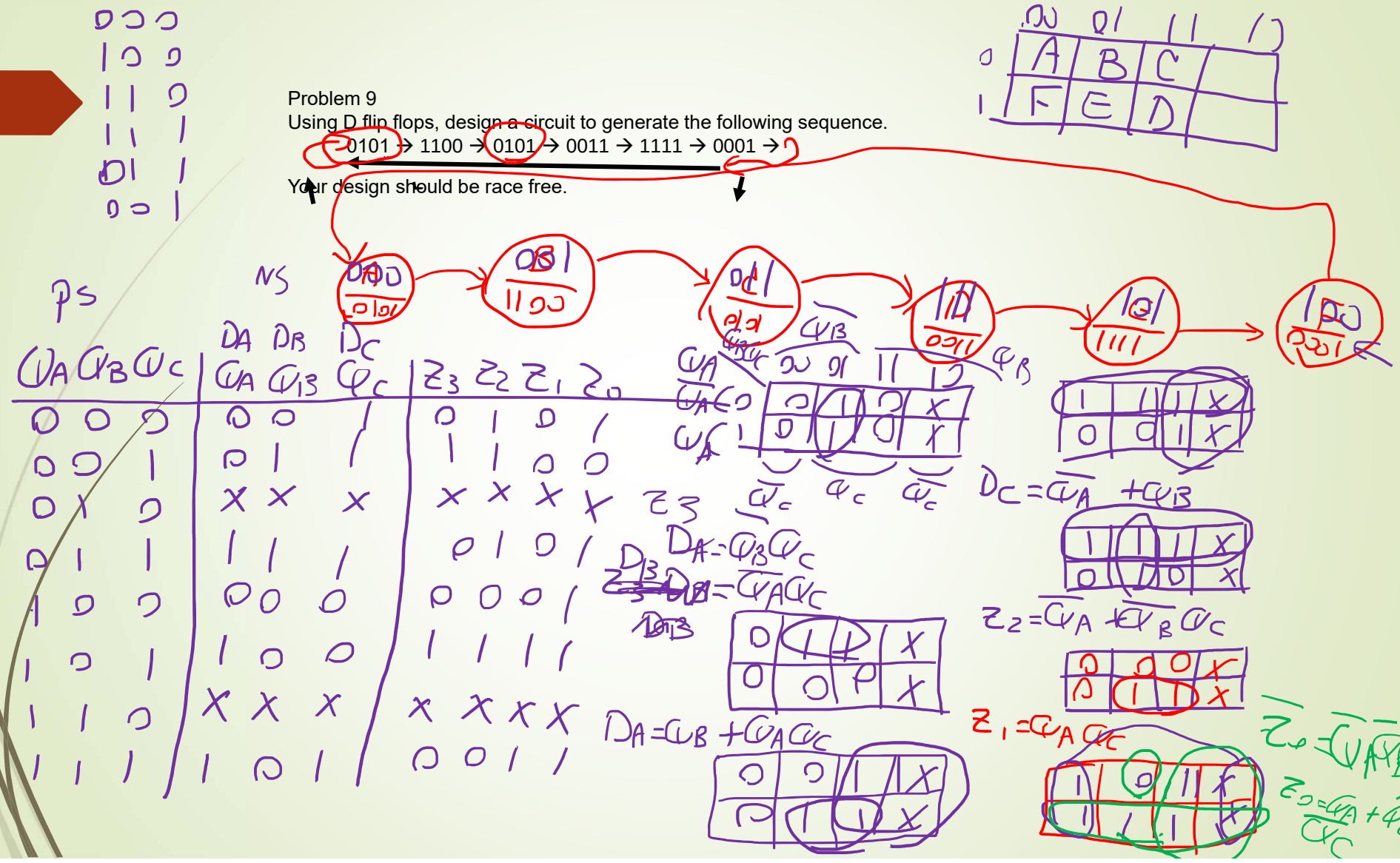
S_1101 : 1101 "

Problem 9

Using D flip flops, design a circuit to generate the following sequence.

0101 → 1100 → 0101 → 0011 → 1111 → 0001 →

Your design should be race free.



$84 - 96 = -12$

84
96
$\leftarrow -96$

S	64	32	16	8	4	2	1
0	1	0	1	0	1	0	0
0	1	1	0	0	0	0	0
1	0	1	0	0	0	0	0

$$\begin{array}{r} 0\,1\,0\,1\,0\,1\,0\,0 \\ +\ 1\,0\,1\,0\,0\,0\,0\,0 \\ \hline (1)\,0\,1\,1\,1\,0\,1\,0\,0 \end{array}$$

2's

NOS.

$$\begin{array}{r} 8\,4\,2\,1 \\ -0000\,1\,1\,0\,0 \\ \hline -12 \end{array}$$

unsigned subtraction

0 1 1 0 1 0

9.5 ← 1 0 0 1 . 1 0

4.25 − 0 1 0 0 . 0 1

```
  1 1 1
  1 0 0 1 . 1 0
+ 1 0 1 1 . 1 1
-----------------
  0 1 0 1 . 0 1
```

(Cy = 1)

$(23.5)_6$

$(34.3)_6$

```
      1 1 5 3
    1 4 3 2
  1 1 5 3
```

$(1\ 3\ 5\ 2.1\ 3)_6$

15 ÷ 6 = 2 R = 3

11 ÷ 6 = 1 R = 5

7 ÷ 6 = 1 R = 1

20 ÷ 6 = 3 R = 2

15 ÷ 6 = 2 R = 3

10 ÷ 6 = 1 R = 4

8 ÷ 6 = 1 R = 2